# Low-Power 1.3-µm VCSEL Transmitter for Data Center Interconnects and Beyond

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**Abstract** *Unprecedented standard single-mode fiber reach of 20km and 4.5km respectively for 28Gb/s and 40Gb/s VCSEL-based intensity-modulation/direct detection optical transmission was obtained with a low-power transmitter assembly including a 4-channel 0.13-µm SiGe driver wire-bonded to a novel 2x1 1.3µm-VCSEL array.*

## Introduction

Long-wavelength vertical-cavity surface emitting lasers (VCSELs) keep attracting more and more attention due to the many advantages associated to their use, i.e. low cost, low power consumption, robustness to high temperatures, potential for hybrid integration on Si-based transceivers and single-mode operation [1-2]. Recent research for optical interconnects mainly focused on 1.5µm VCSEL links achieving data rates up to 56 Gb/s [3,4]. However, chromatic dispersion (CD) of standard single-mode fiber (SSMF) combined with directly-modulated laser chirp, limits the transmission distance to less than 1 km at 40 Gb/s and 500 m at 50 Gb/s [3-6], therefore not matching the fiber reach requirement for large data centers (2 km). The use of the 1.3µm regime would extend the fiber reach, making their use suitable even for inter-data center applications and up to the access segment. Error-free operation through 25 Gb/s directly modulated 1310nm-VCSEL was recently demonstrated up to 10 km of SMF, with data rate limited by the 3dB-modulation bandwidth (11.5GHz) [7]. To enhance the modulation speed, a lot of effort has been recently devoted to both develop dedicated driver circuits implementing feed forward equalization (FFE) [3,5,8] and novel VCSEL designs.

Here we present a transmitter assembly that embeds a novel high-speed 1325nm-VCSEL wire bonded to a low-power SiGe driver circuit including 2-tap FFE, targeting 28 Gb/s and 40 Gb/s over an unprecedented SSMF length.

## 1.3µm-VCSEL description

The single-mode and fixed-polarization VCSEL is based on Vertilas unique Indium Phosphide (InP) Buried Tunnel Junction (BTJ) design. The VCSEL has been optimized for high bandwidth

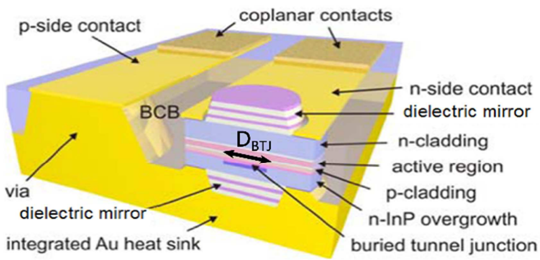


**Fig. 1:** Cross section of short-cavity (SC) VCSEL

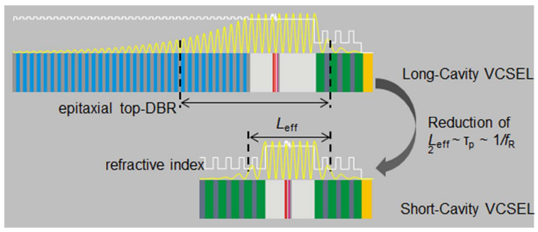


**Fig. 2:** Cavity length of SC and long-cavity VCSEL

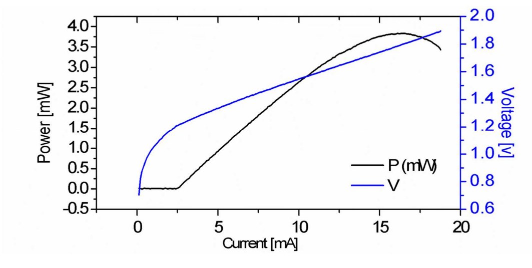


**Fig. 3:** Room temperature output power and diode voltage versus diode current showing threshold current of 2.5 mA and maximum optical power of 3.8 mW with voltage < 1.8 V.

performance with a very short optical cavity reducing the photon lifetime. Both the top and bottom mirror have been realized with dielectric materials, see Fig. 1. The high refractive index of these materials allows to realize the top distributed Bragg reflector (DBR) mirror with only 3.5 mirror pairs, compared with > 30 mirror pairs of an epitaxial DBR mirror. This results in a reduction of the effective cavity length by ca.

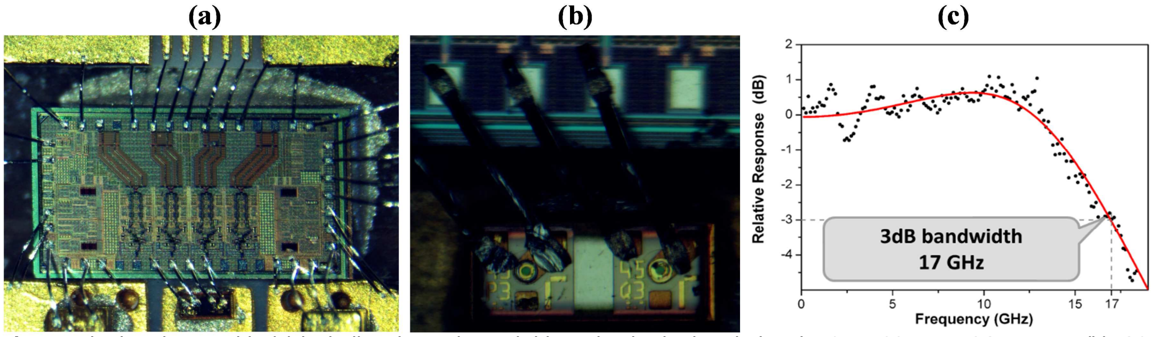

**Fig. 4:** Wire bond assembly (a) including the 4-channel driver circuit wire bonded to the 2x1 1325nm-VCSEL array (b). S21 measurement with corresponding 3dB-modulation bandwidth.

50%, see Fig. 2. In addition, the device parasitics have been further reduced by minimizing the device mesa diameter. The void of the etched area around the mesa is being filled with benzo cyclobutene. Such InP-based VCSEL structure allows single-mode operation with a side mode suppression ratio (SMSR) > 40 dB and 1.3µm wavelength. A maximum optical output power of 3.8 mW is achieved at a roll-over current of 16 mA, while the operating voltage remains below 1.8 V (Fig. 3). The measured 3dB-modulation bandwidth of 17 GHz at room temperature is the highest bandwidth reported for a single-mode 1.3µm-VCSEL, see Fig. 4(c) (in red a 3-pole polynomial fit to black dots raw data).

**Transmitter description and experiment**

The employed transmitter consists of a 0.13µm SiGe BiCMOS 4-channel driver circuit wire bonded to a 2x1 1325 nm-VCSEL array, Fig. 4(a,b). The driver has a footprint of 2.5mm x 1.3mm, channel pitch of 300 µm and operates using a single supply voltage of 2.5 V. The output stage is preceded by a 2-tap FFE driver where magnitude, sign and relative delay of taps can be modified [5]. The reported results refer to the rightmost one of the working channels, see Fig. 4(b). The transmitter has been tested in uncooled condition measuring, through a thermistor, a free-run temperature of ~30°C. At that temperature the VCSEL 3dB-bandwidth was measured to be 15.6 GHz. The differential driver input was fed with a 28 Gb/s data stream whilst only single-ended input drive was possible at 40 Gb/s due to technical limitations. The peak-to-peak voltage of the input ($2^7$-1)-long pseudorandom bit sequence was set at 0.6 V for 28 Gb/s bit rate and at 0.37 V for 40 Gb/s, with applied bias current of 11 mA and 12 mA respectively. Light was coupled out using just a cleaved SMF contacted to the VCSEL output, so as to limit optical reflections. A commercial 40G Linear PIN differential-ended Photoreceiver (DSC-R409-LW by Discovery Semiconductors, Inc.) was employed for bit error rate (BER) and eye diagram measurements. The maximum received optical power was 1 dBm in back-to-back (BTB) configuration with an extinction ratio (ER) of 5.2 dB at 28 Gb/s. Because of the modulation bandwidth limitation and the required stronger equalization, in case of 40 Gb/s data rate a resulting drop of the ER to 2.8 dB was measured and a higher bias current was applied. Eye diagrams including 220 acquired waveforms and corresponding BER curves are shown in Figs. 5-6 for both 28 Gb/s and 40 Gb/s data rates and various SSMF lengths. Error-free operation (BER < $10^{-11}$) was achieved with sensitivity of -10.6 dBm at 28 Gb/s, with 3.3 dB-

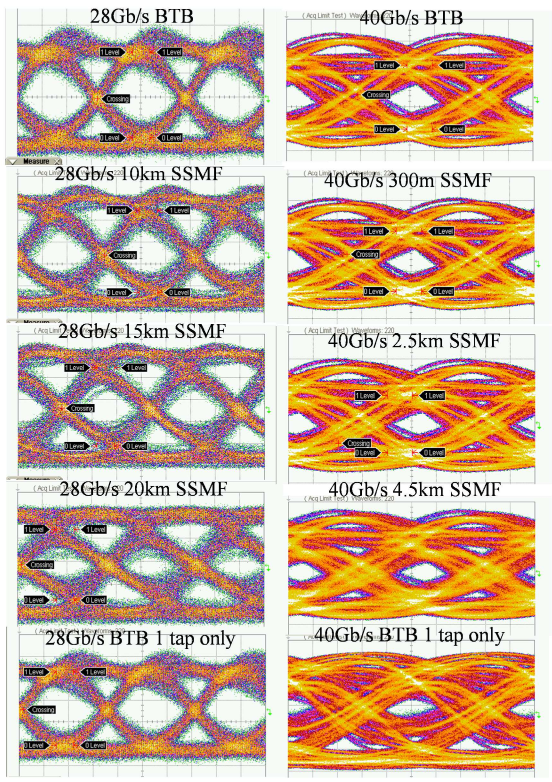

**Fig. 5:** Received eye diagrams at 28 Gb/s up to 20 km of SSMF and at 40 Gb/s up to 4.5 km of SSMF, each diagram made by 220 waveforms. 1-tap FFE case at the bottom for both bitrates.

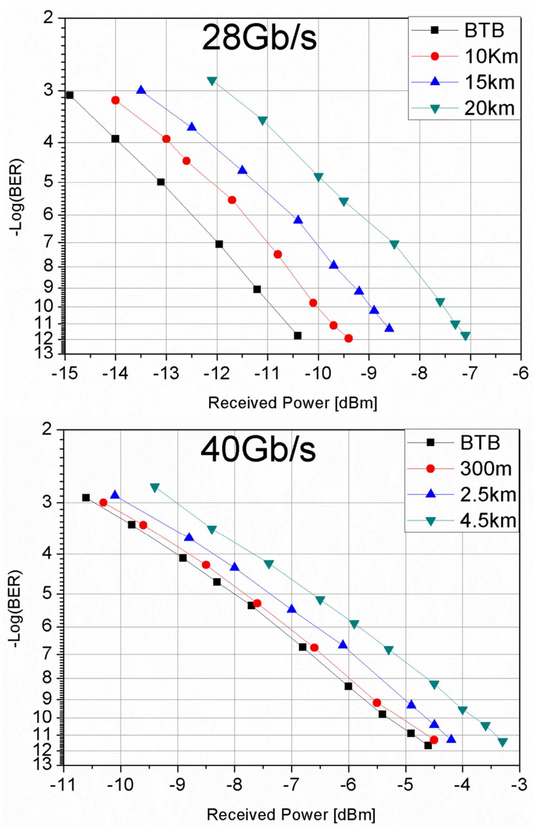


**Fig. 6:** BER curves versus received optical power at both 28Gb/s and 40Gb/s for various SSMF lengths.

power penalty after 20 km of SSMF G.652 and residual power budget of 1.6 dB. The same was achieved with sensitivity of -4.9 dBm at 40 Gb/s, with 1.5 dB-penalty after 4.5 km of SSMF and residual power budget of 3.2 dB. The two bottom eye diagrams of Fig. 5 (FFE with 1 tap only) demonstrate a modest impact of the 2-tap equalization at 28 Gb/s, whereas it was crucial at 40 Gb/s. The different appearance of 40 Gb/s eye diagrams with respect to those at 28 Gb/s is due to the use of a precision timebase module (Agilent 86107A) for clock triggering, which leaded to a much longer time (minute range) required to acquire 220 waveforms. The employed sampling oscilloscope for eye diagrams visualization was an Agilent 86100A (50G 86109B module) and the error analyzer for BER measurement was a SHF 11100A. The measured power consumption of the whole assembly was ~190 mW, of which 170 mW was consumed by the driver and FFE and ~20 mW was required for VCSEL biasing. This translates into an energy-per-bit of 4.75 pJ/bit at 40 Gb/s being significantly better than [3] and [8], where similar FFE-drivers were used. In addition, the potential of the presented 1.3µm BTJ VCSEL for data center and inter-data center traffic is strongly supported by comparing its efficiency with respect to similar solutions, through the energy-to-data-ratio per km, as figure of merit. Error-free and digital signal processing (DSP)-free transmission at 28 Gb/s over 20 km of SSMF leads to 29 fJ/bit/km, whereas in [7] 119 fJ/bit/km at 25 Gb/s over 10 km of SMF can be deduced and in [9] 57 fJ/bit/km are required excluding DSP power consumption to achieve a BER < $10^{-6}$ at 28 Gb/s over 10 km of SSMF.

## Conclusions

This work has demonstrated that 1.3µm-VCSEL transmitters for data center interconnects are capable of transmitting over distances multiple times longer than using 1.55µm devices [3-6,9]. The achieved results, in particular error-free (BER < $10^{-11}$) transmission at 28 Gb/s over 20 km of SMF G.652 and at 40 Gb/s over 4.5 km of the same fiber type, with neither forward error correction (FEC) nor DSP, exceed the long-wavelength VCSEL state of the art and make the proposed transmitter assembly compliant with the IEEE 802.3 100GBASE LR4 standard. In addition, the 4-channel driver wire bonded to a quad VCSEL array has the potential to establish a 100 or 160 Gb/s VCSEL link.

## Acknowledgements

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